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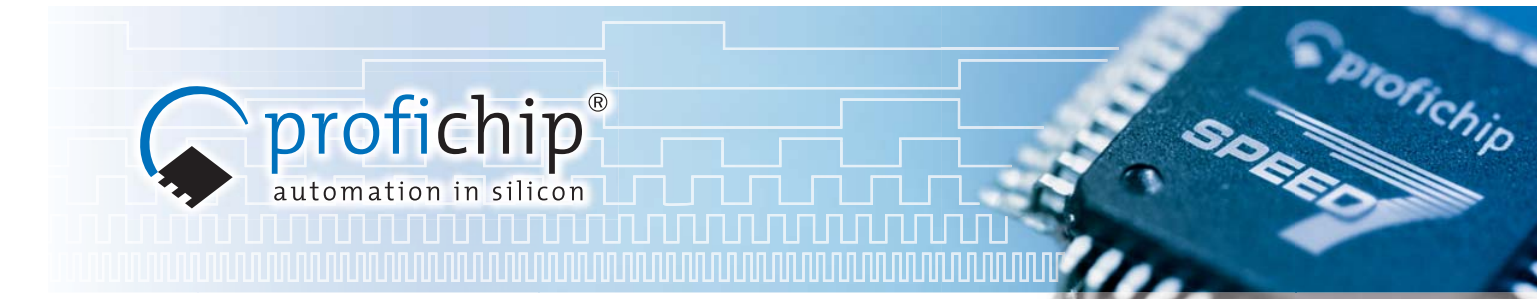
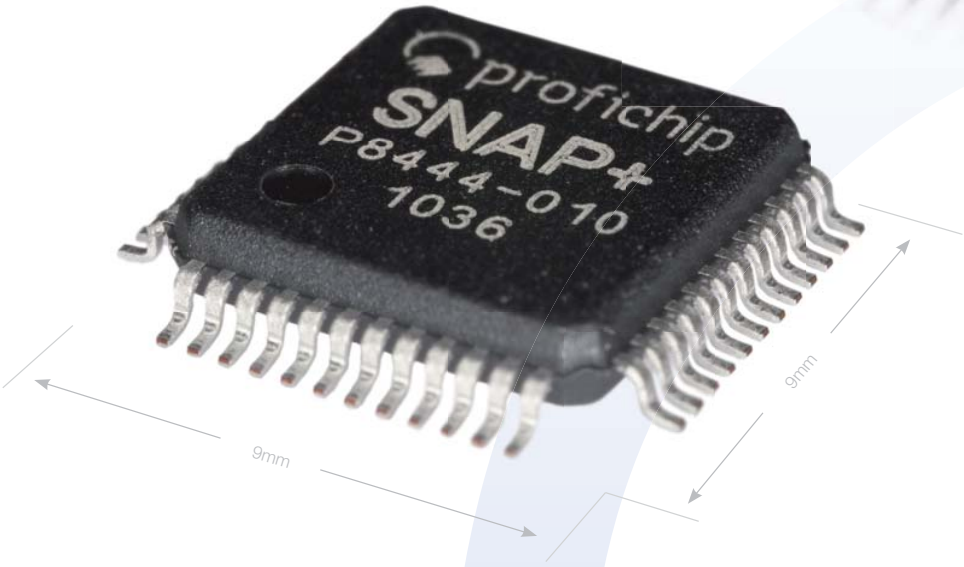
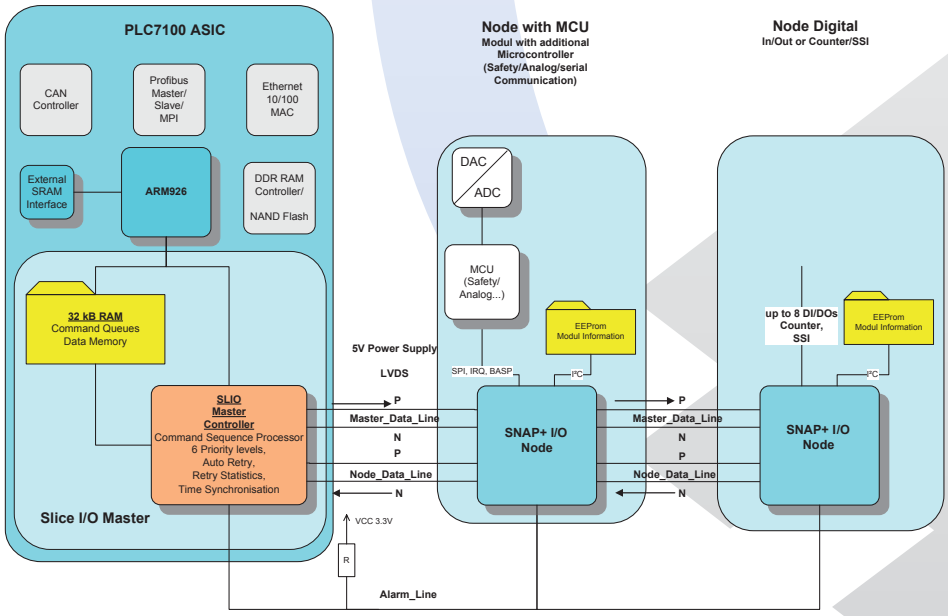




I/O Backplane Controller for high speed Remote I/O

SNAP+



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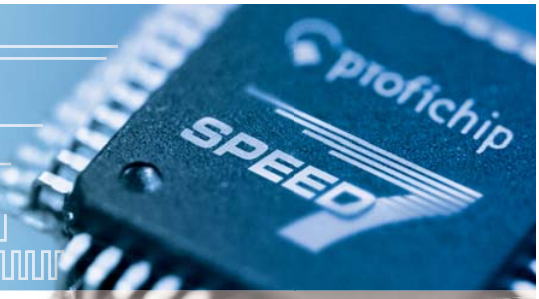

Basic SLIO backplane bus Information:
- Single master system
- Up to 64 slave (Node) stations
- Asynchronous, serial data transmission with 48 MBit/s over Point to Point LVDS physic
- Additional alarm line for initialization and asynchronous event communications from node to master
- Full system detection from SLIO master without external information on module configuration

Error detection mechanism:
- CRC code with Hamming distance 4 for every telegram (all 3 bit errors will be detected)
- Watchdog function inside every node for SLIO master observation
- “Auto shut down” in case of SLIO master malfunction
- Retry statistic for early detection of possible transmission issues

Time-synchronisation:
- Every node has its own clock with 1µs resolution
- All node clocks are synchronized with the SLIO master (accuracy <100ns)
- Option for clock synchronization from SLIO master to SLIO master via different protocols (Profibus DP V2, Profinet, Ethercat,...)

Technological functions in SNAP+:
- Standard I/O function: 8 digital I/O or up to 32 I/O with shift register
- Integrated digital input filter function
- Asynchronous event signaling with µs time stamping for advanced nodes
- Two advanced counters with AB oversampling, latch, reset, output, hysteresis, comparevalue, repetitive/endless counting and additional time stamp information
- SSI function with time stamp information (speed calculations: counter difference/time)
- Pulse Width Modulation with 20ns resolution
- Frequency measurement mode
- Special digital I/O time stamp nodes (ETS: Edge Time Stamp System) for input edge and output control with 1µs resolution (independent from fieldbus cycle!)

SPI interface in SNAP+ for analog I/O / safety / serial CP with external MCU:
- 3 MBit/s SPI interface for external microcontroller
- Up to 192 Byte for parameters, up to 16 Byte In / 16Byte Out data for external microcontroller
- Alarm function and watchdog function

Performance:
- Different „Speed Grades“ for data transmission
- Multinode telegrams for maximum efficiency:
  - Write 64 nodes (8 outputs/node): 17µs
  - Read 64 nodes (8 inputs/node): 32µs (with node presence check)
- Asynchronous event reaction time: 9µs

Mechanical and electrical specification SNAP+ (preliminary):
- I/O voltage: 3,3V, typ. 16mA, core voltage: 1,8V, typ. 16mA
- DI8 or DO8 modul without I/O load: typical: 5V, 32mA
- LQFP 48 package, 9,0mm², pitch 0,5mm

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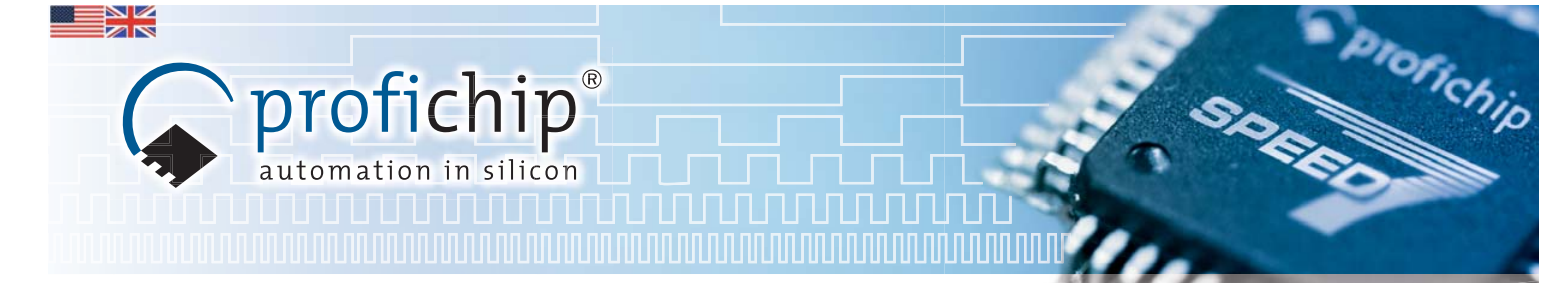
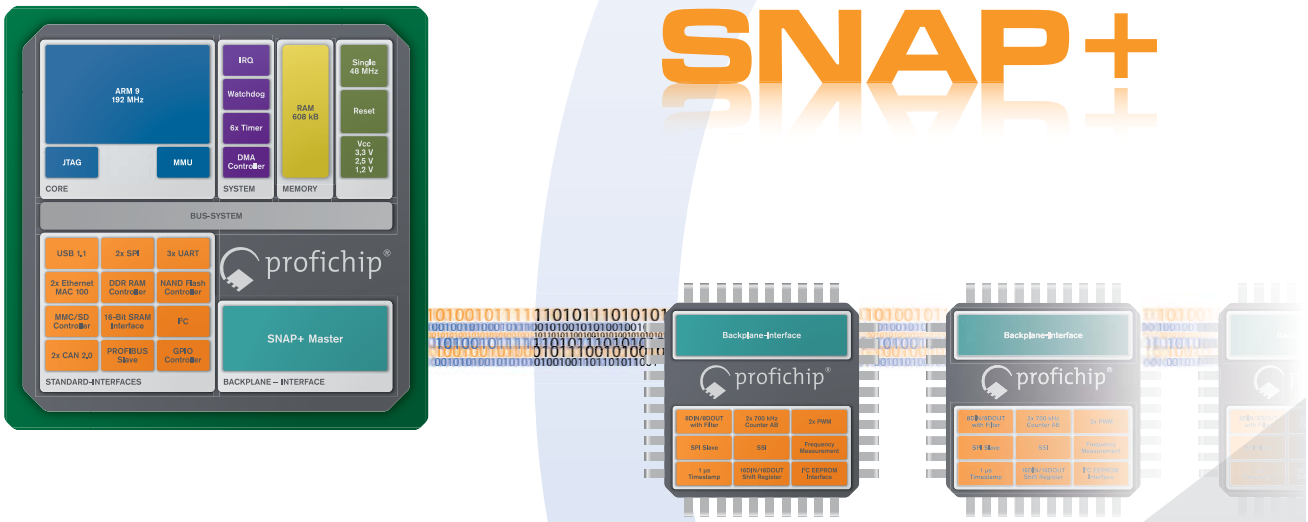


SliceBus Technology
Industrial Backplane Chipset
SMC1000

SNAP+



Performance and flexibility …

- High speed communication for modular systems
- Ready-to-use chipset
- Outstanding noise immunity, detailed diagnostics and smart error handling
- Easy expansion up to 64 nodes
- Flexibility for multiple fieldbus couplers and interfaces
- Integrated technology functions reduce total system cost
- Easy-to-use accurate time synchronization

… build your own system!

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Basic SliceBus Information

- SMC1000 single master system
- Up to 64 SNAP+ slave stations
- 48 Mbit/s LVDS physic
- Additional alarm line for initialization and asynchronous event communication from node to master
- Master identifies and addresses all nodes autonomously

Error detection mechanism

- CRC code with Hamming distance 4 for every telegram (all 3 bit errors will be detected)
- Watchdog function inside every SNAP+ slave for master observation.
- SNAP+ “Auto shut down”

Time-synchronisation

- Every SNAP+ with internal 1 µs resolution clock
- Slave synchronization with SMC1000 master (accuracy < 100 ns)
- SMC1000 master to master clock synchronization option for most industrial fieldbus protocols (PROFIBUS DP V2, PROFINET, EtherCAT,...)

SMC1000 Master main features

- ARM926 core
- Integrated PROFIBUS slave interface (VPC3+) with data rates up to 12 Mbit/s
- 2 Fast Ethernet (10/100 Mbit/s) MACs with 2kB of independent transmit and receive buffers each
- 2 CAN interfaces
- 3 fast UARTS, 2 SPI channels, I²C Interface
- USB 1.1 full speed device endpoint with PHY
- Configurable 8 bit/16 bit asynchronous SRAM Interface
- DMA capable 8 bit NAND Flash Controller
- MMC/SD Card Controller
- 8 priority level advanced IRQ controller
- 16 bit DDR-RAM Controller
- 608 kB internal SRAM

SNAP+ Technological functions

- Standard I/O function: 8 bit digital I/O or up to 16 bit digital I/O with shift register
- Advanced counters with additional time stamp information
- SSI function with time stamp information (speed calculations: counter difference/time)
- Pulse Width Modulation with 20 ns resolution
- Frequency measurement mode with up to 600 kHz resolution
- Special digital I/O time stamp nodes (ETS: Edge Time Stamp System) for input edge and output control with 1 µs resolution (independent from fieldbus cycle!)

SPI slave interface in SNAP+

- for applications that need an external MCU, like analog I/O, Safety or serial CPs
- 2.6 Mbit/s SPI interface
- Up to 180 Byte for parameters, up to 16 Byte In / 16 Byte Out data for external microcontroller
- Alarm function and watchdog function

Performance (maximum values)

- Write 64 nodes (8 outputs/node): 17 µs
- Read 64 nodes (8 inputs/node): 32 µs (with node presence check)

Package

- SNAP+: LQFP 48, pitch 0.5 mm, 9x9 mm²
- SMC1000: PBGA 324, pitch 1.0 mm, 19x19 mm²